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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,761	11/21/2003	Atsuhiko Amagami	JP920020198US1	3102

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EXAMINER	
SUN, SCOTT C	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 06/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,761	AMAGAMI, ATSUHIKO	
	Examiner	Art Unit	
	Scott Sun	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/28/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claim 22 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Specifically, a computer program per se is not statutory.

3. To expedite a complete examination of the instant application, the claim(s) rejected under 35 USC 101 (non-statutory) above are further rejected as set forth below in anticipation of applicant amending these claims to place them within the four statutory categories of invention.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Francis James Canova (JP 04-248609, IDS filed 11/28/2005).

6. Regarding claim 1, 9, and 19, Canova discloses an apparatus (system in figure 1) comprising: a first terminal (ID pin 1) at which a first identification signal (low signal

output from ID pin 1) which forms a part of device identification information is output; a second terminal (ID pin 0) at which a first change signal (a low level signal is input to ID pin 0) is received which directs a change in the output from said first terminal (ID pin 1 subsequently outputs a high); and an output setting circuit (internal circuitry inside device 103) operatively connected with said first and second terminals and directing that a second identification signal (signal output from ID pin 1 after low level signal is written to ID pin 0) which forms a part of the device identification information be output from said first terminal in a state in which said first change signal has been input to said second terminal (paragraph 8). Examiner notes that Canova teaches that the identification information is read in a 3-stage process containing a first read, a write, and a second read from the ID pins. Based on the identification circuitry on the device to be identified, the signals derived from the first and second read commands form the identification information. Canova also discloses different examples in figures 2-7 of using only 2 ID pins to represent 7 different identification numbers.

Further regarding claims 1 and claim 19, Canova further discloses a first acquisition element (tri-state buffers 402:0 and 402:1) which acquires from another device a first identification signal output at a first terminal of the other device (paragraph 6); a second acquisition element (D flip-flops 403:0 and 403:1) which acquires from the other device a second identification signal output at said first terminal in a state in which a first modification signal directing change to the signal output at said first terminal is output to a second terminal of the other device (paragraph 7, 8); an identification information determining element (CPU 410) which determines information identifying

the other device based on the acquired first and second identification signals (paragraph 8). Examiner notes that Canova teaches the tri-state buffers read the ID pin values from the initial read cycle. In the subsequent write cycle, the one of the D flip-flops output a low signal to the ID pin that originally output a high signal, causing a new identification signal to be read the other ID pin.

7. Regarding claim 10, Canova discloses the apparatus according to claim 9, and further discloses wherein: said second terminal outputs a third identification signal (signal read on ID pin 0 during first read) forming a part of the device identification information; and said output setting circuit causes said second identification signal to be output from said first terminal in a state in which said first change signal having a value different from the signal value of said third identification signal has been input through said second terminal (paragraph 8). Canova teaches that a low signal (interpreted as signal directing change) is written to the ID pin that originally output a high.

8. Regarding claim 11, Canova discloses the apparatus according to claim 10, and further discloses wherein: said output setting circuit inputs the signal value of said second terminal, and, in a state in which said second terminal has the signal value of said third identification signal, outputs said first identification signal to said first terminal, and, in a state in which said second terminal has the signal value of said first change signal, outputs said second identification signal to said first terminal (paragraph 8, see examiner's remarks for claims 9 and 10 above).

9. Regarding claim 12, Canova discloses the apparatus according to claim 10, and further discloses wherein: said output setting circuit has wiring for providing electrical connection between said first and second terminals (wire in figure 1, paragraph 8).

10. Regarding claim 13, Canova discloses the apparatus according to claim 12 further comprising a pull-down portion (NOT gate 110) for said second terminal pulled up by a first resistor (pull up resistor 401:0; paragraph 8), and pulling down said second terminal by a second resistor having a value lower than that of said first resistor.

11. Regarding claim 14, Canova discloses the apparatus according to claim 10, and further discloses wherein: wherein said output setting circuit outputs the logical negation value of the signal value of said second terminal to said first terminal (see rejection for claim 13).

12. Regarding claim 15, Canova discloses the apparatus according to claim 10, and further discloses wherein: wherein said output setting circuit has a combinational logic circuit (NAND gate in figure 9) for outputting the result of a logical operation on the signal values of plurality of said second terminals to said first terminal. Examiner notes that Canova teaches the 3-pin example of the identification system in which output of 1 pin is a logical combination (in the example, NAND) of values of two other pins.

13. Regarding claim 16, Canova discloses the apparatus according to claim 10, and further discloses wherein: wherein said output setting circuit has an open-collector logic (transistor shown in device figure 1) output or open-drain logic output for outputting said first or second identification signal to said first terminal.

14. Regarding claim 17, Canova discloses the apparatus according to claim 10, and further discloses wherein: wherein said output setting circuit has a rectifier for preventing backflow of a current from said first terminal to said second terminal. Examiner asserts that one of ordinary skill in the art would recognize a rectifier or equivalent circuit is needed to maintain the signal outputs of the respective ID pins.

15. Regarding claim 18, Canova discloses the apparatus according to claim 9, and further discloses wherein: further comprising a third terminal (ID pin 2) connected to a predetermined potential for outputting said predetermined potential as at least part of said first identification signal forming a part of said identification information (figure 9, paragraph 26, 27)

16. Claims 2-8 and 20-22 are substantially similar to claims ~~1-9-18~~ 10 - 18 above. They are rejected under the same grounds of rejection.

17. Other publications are cited to further show the state of the art with respect to device identification. Refer to form 892, "Notice of References Cited", for a complete list of relevant prior arts cited by the examiner.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Sun whose telephone number is (571) 272-2675. The examiner can normally be reached on M-F, 10:30am-7pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim N. Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

5/10/2006

KIM HUYNH
SUPERVISORY PATENT EXAMINER

5/11/06